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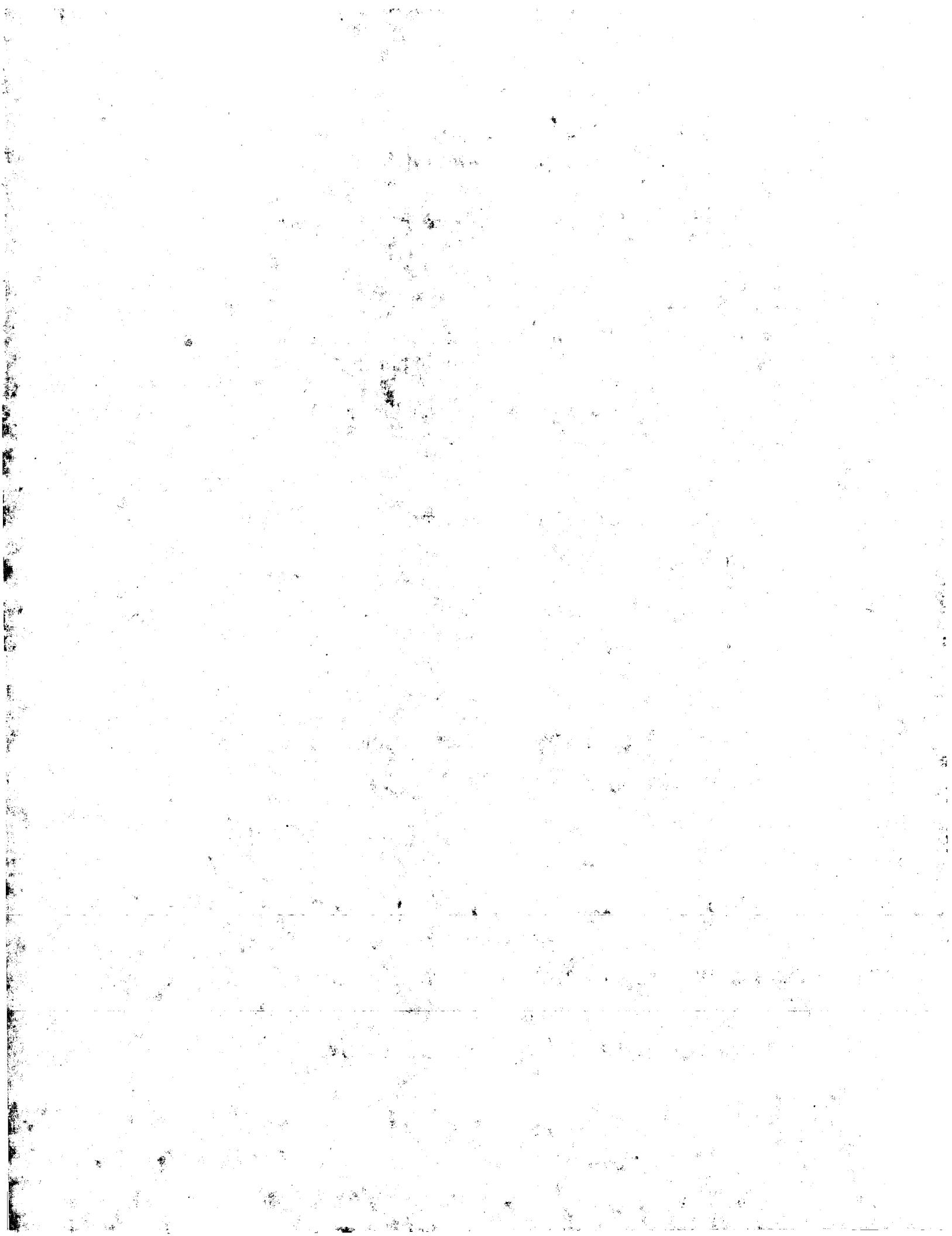
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10828712

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
22 March 2001 (22.03.2001)

PCT

(10) International Publication Number
WO 01/20664 A1

(51) International Patent Classification⁷: H01L 21/76, 27/04, 29/06

(21) International Application Number: PCT/SE00/01690

(22) International Filing Date:
4 September 2000 (04.09.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
9903338-3 17 September 1999 (17.09.1999) SE
0000296-4 28 January 2000 (28.01.2000) SE

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(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

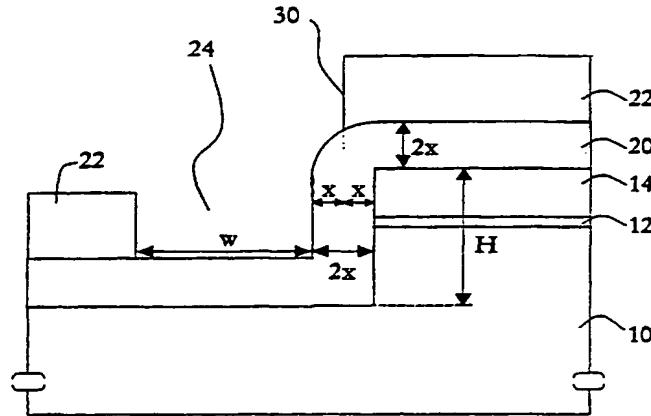
(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:

— With international search report.
— Before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments.

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: A SELF-ALIGNED METHOD FOR FORMING DEEP TRENCHES IN SHALLOW TRENCHES FOR ISOLATION OF SEMICONDUCTOR DEVICES



WO 01/20664 A1

(57) Abstract: In the fabrication of an integrated circuit, particularly an integrated circuit for radio frequency applications, a method for forming shallow and deep trenches for isolation of semiconductor devices comprised in said circuit, comprising providing a semiconductor substrate (10); optionally forming a first dielectric layer (14) on said substrate; forming at least one shallow trench (18) by using a first mask (16), said shallow trench extending into said substrate; forming a second dielectric layer (20) of a predetermined thickness (2x) on the structure obtained subsequent to the step of forming at least one shallow trench; forming at least one opening (33) in said second dielectric layer by using a second mask (22) with an edge (30) of said second mask aligned to an edge (26) of said shallow trench with a maximum misalignment (+/- x) of half the predetermined thickness (2x), said opening extending with the shallow trench to the bottom (18a) thereof, whereby a spacer (32) of a width equal to the predetermined thickness (2x) is formed in said shallow trench and along said edge thereof; and forming a deep trench (34) in said opening by using said second dielectric layer as a hard mask, said deep trench extending further into said substrate and being self-aligned to said shallow trench.

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A SELF-ALIGNED METHOD FOR FORMING DEEP TRENCHES IN SHALLOW TRENCHES FOR ISOLATION OF SEMICONDUCTOR DEVICES

TECHNICAL FIELD OF THE INVENTION

The present invention generally relates to the isolation of semiconductor devices in integrated circuits by using isolation structures, thus enabling increase of the packing density and isolation.

More specifically, the invention relates to a method for fabrication of a semiconductor structure comprising a shallow isolation region and a deep trench isolation region, to the semiconductor structure itself, and to an integrated circuit comprising such a semiconductor structure.

DESCRIPTION OF RELATED ART

All non-trivial integrated electronics involves connecting isolated devices through specific electrical connection paths.

The device isolation scheme is therefore one of the critical parts when fabricating integrated circuits. Many different schemes have been developed during the years. Parameters like minimum isolation spacing, surface planarity, defect density, process complexity and electrical properties, i.e. DC and high frequency properties, influence the choice of a scheme for the particular application and process technology. Mesa isolation, junction isolation and LOCOS (local oxidation of silicon) isolation are common techniques in use, see e.g. Chapter 2 in S. Wolf, "Silicon Processing for the VLSI ERA, Volume 2 - Process integration", Lattice Press, Sunset Beach, 1990.

As feature sizes in modern, high-complexity integrated circuits (ULSI, ultra large scale integration) decreases, there is a need to reduce shortcomings, such as packing density, leakage currents and latch-up between devices, associated with older isolation technologies. Shallow and deep trench isolations have therefore become very popular. Although demanding on the

etching and refilling process steps, they offer vast improvement in decreased area needed for the isolation between circuit elements and e.g. storage capacitors in DRAM memory technologies.

5 The trenches are formed by removing silicon by dry etching and filling them with suitable dielectric or conductive materials. Shallow trench isolation (STI), which is used to replace LOCOS isolation, usually has a depth of a few tenths of a micron and is used for isolation between device elements. Shallow trench
10 isolation is closer described in e.g. "Choices and Challenges for Shallow Trench Isolation", Semiconductor International, April 1999, p. 69. Deep trenches, usually with a depth larger than a couple of microns, are mainly used to isolate different devices and device groups (wells) in CMOS/BiCMOS technology, to
15 form vertical capacitors and to form high-conductive contacts to the substrate, see C. Y. Chang and S. M. Sze (Eds); "ULSI Technology", McGraw-Hill, New York, 1996, pp. 355-357 and WO 97/35344 (inventors: Jarstad and Norström). The trenches are filled with oxide, polysilicon or other materials, and the
20 surface is planarised, either by dry etching or by chemical mechanical polishing (CMP).

In U.S. patent 4,994,406 issued to Vasquez and Zoebel is described a method to form shallow and self-aligned deep isolation trenches on an integrated circuit. Although the deep
25 trench are being self-aligned to the edge of the device areas, the structure uses a polysilicon nitride stack to form device isolation using LOCOS, with large lateral encroachment, high temperature budget, and a non-planar surface as a result.

U.S. patent 5,691,232 issued to Bashir discloses a method to
30 form shallow and deep trench isolation by combining the formation of the two. First, a shallow trench is formed using a first mask, and then a deep trench is formed using a second mask. The whole structure is filled with oxide and planarised.

Since the mask for the deep trench must be aligned against the mask for the shallow trench, less packing density is achieved and/or leakage current problems will occur when the structure is scaled. Also, filling of narrow deep trenches usually 5 requires the use of polysilicon and back etching, not included in this description.

In U.S. patent 5,895,253 issued to Akram is described a method to form a deep trench within a shallow trench and how to fill it with an insulator. The deep trench is self-aligned within the 10 shallow trench. This is made with only one mask step. After forming the trench, it is filled in a common way. Although the patent teaches how to place a deep trench self-aligned within the shallow trench, the method uses only one mask step, and it will not be possible to use shallow trenches without any deep 15 trench. The width of the deep trench is set by the width of the shallow trench opening and spacer widths. If different shallow trench openings are used, the etching and filling of the deep trenches will become difficult or even impossible.

SUMMARY OF THE INVENTION

It is consequently an object of the present invention to provide 20 a method in the fabrication of an integrated circuit, particularly an integrated circuit for radio frequency applications, for forming shallow and deep trenches for isolation of semiconductor devices comprised in said circuit, while overcoming at least some of the problems associated with 25 the prior art.

It is a further object of the invention to provide a fabrication method that permits deep trenches to be placed inside shallow trench regions, with adjustable distance from 30 the edge of the shallow trench to the deep trench, still allowing the formation of shallow trench areas without any deep trenches inside.

It is yet a further object of the invention to provide such a method having enhanced scalability characteristics enabling an increased packing density.

5 It is still a further object of the invention to provide such a method having increased integration flexibility and which is compatible with several technologies.

These objects among others are, according to one aspect of the invention, fulfilled by a method comprising the following steps:

- providing a semiconductor substrate;
- 10 - optionally forming a first dielectric layer on said substrate;
- forming at least one shallow trench in said first dielectric layer or in said substrate by using a first mask formed on said first dielectric layer, said shallow trench extending into said substrate;
- 15 - forming a second dielectric layer of a predetermined thickness, $2x$, on the structure obtained subsequent to the step of forming the at least one shallow trench;
- forming at least one opening in said second dielectric layer by using a second mask formed on said second dielectric layer and with an edge of said second mask aligned to an edge of said shallow trench with a maximum misalignment of half the predetermined thickness of said second dielectric layer, i.e. $+/- x$, said opening extending within the shallow trench to the bottom thereof, whereby a spacer of a width equal to the predetermined thickness, $2x$, is formed in said shallow trench and along said edge thereof; and
- 20 - forming a deep trench in said opening by using said second dielectric layer as a hard mask, said deep trench extending further into said substrate and being self-aligned to said shallow trench.
- 25
- 30

Furthermore it is an object of the present invention to provide a semiconductor structure resulting from above said fabrication method.

According to a second aspect of the present invention there is thus provided a semiconductor structure comprising a semiconductor substrate; at least one shallow trench extending vertically into said substrate; a deep trench laterally within said shallow trench, said deep trench extending vertically further into said substrate, wherein said deep trench is self-aligned to said shallow trench with a controlled lateral distance between an edge of the shallow trench and an edge of the deep trench, and the lateral extensions of the shallow and deep trenches, respectively, are independently chosen.

An advantage of the present invention is that the distance between the deep and shallow trench edges is fixed and determined by the thickness of the deposited second dielectric layer, thus easily controllable.

Another advantage of the invention is that the distance between the deep and shallow trench edges is minimized in order to obtain an increased packing density of the integrated circuit, still providing a step between them in order to prevent stress arising from deep trench processing to interfere with active areas.

Further advantages and characteristics of the present invention will be disclosed in the following detailed description of embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more fully understood from the detailed description of embodiments of the present invention given hereinbelow and the accompanying Figs. 1-11 which are

given by way of illustration only, and thus are not limitative of the invention.

5 Figs. 1-3 and 5-8 are highly enlarged cross-sectional views of a portion of a semiconductor structure during processing according to the present invention.

Fig. 4 is a view from above of a portion of a semiconductor structure during processing according to the present invention.

10 Figs. 9-11 are SEM images of cross-sections of a portion of a semiconductor structure during processing according to the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS

In the following description, for purposes of explanation and not limitation, specific details are set forth, such as particular hardware, applications, techniques, etc. in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced in other embodiments that depart from these specific details. In other instances, detailed descriptions of well-known methods, protocols, devices, and circuits are omitted so as not to obscure the description of the present invention with unnecessary details.

20 With reference to Figs. 1-11 an inventive embodiment of a process sequence, which includes formation of shallow and deep trenches, filling of the trenches and planarisation, is described in detail.

Prior to formation of isolation, sub-collectors, wells or any other device regions may have been formed in the starting material. However, at the stage where the present inventive process is to be started, the surface of a silicon substrate is 30 clean and any layers on top of the silicon have been removed.

With reference to Fig. 1 the formation of a hard mask for a shallow trench is described. The masking layer for the shallow trench is formed by oxidizing silicon surface 10 to form a layer 12 of thermal silicon dioxide of typically 100 Å thickness.

5 Next, an approximately 2000 Å thick silicon nitride layer 14 is deposited by chemical vapor deposition (CVD). Other combinations of thicknesses and/or masking materials are possible.

With reference next to Fig. 2, the formation of a shallow trench is considered. A photo resist 16 is applied on the nitride layer 14, and is exposed using a first mask, so called moat mask, which leaves openings where the shallow trench is to be etched.

10 The etching, which preferably is non-isotropic, is performed by reactive ion etching (RIE), through the nitride/oxide layers 12, 14 and into the silicon substrate 10 to form a vertical shallow trench 18. The preferred depth of trench 18 is 0.2-0.7 µm, or more typically 0.3-0.6 µm, from the silicon surface 10a. The photo resist 16 is removed subsequent to the etching of shallow trench 16.

20 With reference next to Figs. 3 and 4 the formation of a hard mask for a deep trench is described.

25 A silicon oxide layer 20 of thickness $2x$ is deposited, preferably conformly, e.g. by CVD, on top of the structure, i.e. remaining portions of the nitride layer 14 and in the shallow trench 18. It is preferred that the oxide layer 20 is deposited conformly as otherwise margins for subsequent masking and etching will be reduced. Photo resist 22 is applied, and is exposed using a second mask, so called trench mask, which, together with portion of oxide layer 20, define an opening 24 with a width w for the deep trench.

30 The layouts of the first and second masks, respectively, are illustrated in Fig. 4, which shows the semiconductor structure from above. The edges of the shallow trench and of the opening

that will constitute the lateral definition of the deep trench are indicated by 26 and 28, respectively.

The opening(s) of the trench mask may be placed anywhere inside the shallow trench regions. The width of the deep trench can be chosen by using different mask dimensions. It is usually preferred to use trenches of fixed lateral dimensions (thicknesses), preferably of about 1 μm or less, as problems otherwise will occur with a non-uniform etch and difficulties to refill and planarise the deep trench.

One feature of the present invention is the alignment of the mask edge 30 to the shallow trench edge 26, which makes it possible to place the deep trench self-aligned with a distance set by the oxide thickness $2x$, which in a preferred example is between 1000 and 4000 \AA , and typically 2500 \AA .

Preferably, the height H of shallow trench 18, oxide layer 12 and nitride layer 14 (i.e. the total etching depth when forming shallow trench 18) and the thickness $2x$ of silicon oxide layer 20 fulfill the following relation:

$$H > 2x$$

In Figs. 3 and 4 are shown the details of the mask alignment and the oxide thickness. Assuming that the oxide is 100% conform (uniform in thickness at steps) with a thickness of $2x$, the trench mask 30 is positioned with an overlap x from the silicon nitride edge 26, which position was given by the moat mask. A modern stepper can align the mask with a precision better, or even much better, than 1000 \AA .

Next with reference to Fig. 5 the formation of an oxide spacer 32, is considered. The oxide layer 20 is etched by reactive-ion etching (RIE) to define the trench opening 33 extending to the bottom surface 18a of the shallow trench. Simultaneously, sidewall oxide spacer 32 at the shallow trench edge is formed

of portion of layer 20, which has a width of $2x$. By controlling the oxide thickness $2x$, the distance from the shallow trench edge to the deep trench opening can be adjusted. On top of the nitride layer 14, the oxide layer 20 is protected by the photo resist mask, and this oxide will later serve as a hard mask for these areas during the following etch step. The oxide layer 20 also is retained at portions of the shallow trench area, where no deep trenches will be formed. After etching the photo resist is removed.

With reference next to Fig. 6, a deep trench 34 is formed by etching, using the oxide layer 20 and the spacer 32 as a hard mask. The oxide spacer 32 of width $2x$ defines the distance from deep trench 34 to the active area. The depth of the deep trench is at least a few microns, and more preferably at least 5 microns.

With reference now to Fig. 7, the oxide hard mask 20, 32 for the patterning of the deep trench 32 is removed in e.g. HF.

Subsequent filling and planarisation of trench areas can be accomplished in several ways known from the literature. As an illustrative example, the processing is continued by performing a liner oxidation, which purpose is to perform corner rounding at the sharp edge of the trenches, in order to reduce stress and unwanted electrical effects. This is accomplished by growing a thin ($200\text{--}300\text{ \AA}$) thermal oxide 36 at high temperature ($>1000\text{ }^{\circ}\text{C}$). Since the spacer has been removed, a small "bird's beak" 38 will be formed in the oxide layer 12 under the nitride layer 14, which will further add to the corner rounding, see Fig 7.

Next, with reference to Fig. 8, the trench is filled in a conventional manner with a 2000 \AA thick layer 38 of TEOS and with 15000 \AA of polysilicon 40. The polysilicon is then etched back to remove all polysilicon from the shallow trench areas.

Alternatively, the polysilicon is planarised by chemical mechanical polishing before the polysilicon is etched back from the shallow trench areas. Hereby, the recess of the polysilicon 5 fill in the deep trench is reduced. Consequently, a thinner oxide can be deposited in the subsequent step to fill the shallow trench.

Alternatively, a dielectric is used to fill the trenches instead of polysilicon. Finally, the remaining shallow trench 10 is filled with e.g. CVD oxide 42 or a high density plasma (HDP) oxide, and planarised, either by dry etching methods or by chemical mechanical polishing. The resulting structure is shown in Fig. 8. The processing continues further with forming of the active devices etc., which is not shown in the Figures, and 15 will not be further described in this description.

With reference next to Figs. 9-11, SEM (scanning electron microscope) images of cross-sections of a portion of the semiconductor structure during processing according to the present invention will be briefly discussed.

20 Structures as obtained prior to trench filling are shown in Figs. 9 and 10. Note that the oxide/nitride layers on top are not distinctly visible. In Fig. 9 the scanning electron micrograph shows shallow trench areas without any deep trench (left-most and right-most structures) and another shallow trench 25 area with two deep trenches self-aligned to the edges of the shallow trench area (in the middle). The framed area indicated by 44 corresponds to the structure shown in Figs. 1-3 and 5. In Fig. 10 the micrograph shows device areas 46 for two bipolar transistors 48, 50 as indicated in the Figure, where the deep 30 trench close to the collector contact area 52 is self-aligned to the shallow trench isolation edge.

Finally, Fig. 11 shows a SEM image of the structure subsequent to the back etching when the polysilicon is removed from the shallow trench areas. In the Figure the structures resulting from the etching are indicated by 54 and the 2000 Å thick TEOS layer on top of the nitride/oxide layers and in the trench areas is indicated by 56.

In summary, the present invention uses an additional mask (trench mask) step and makes it compatible with shallow trench isolation, to create a planar surface. Deep trenches may be placed anywhere within shallow trench areas. Furthermore, by forming an oxide spacer at the shallow trench step, the deep trench can be formed self-aligned to the shallow trench. The distance from the deep trench to the active area is controlled by the hard mask oxide thickness. This maximizes packing density and prevents the trench from reaching active areas, which may lead to leakage currents, reduced breakdown voltage or other unwanted effects.

Thus, the present invention exhibits i.a. following advantages:

- The STI overlap between deep trench and active device areas (i.e. distance between deep trench edge and shallow trench edge, 2x) is minimized and easily controllable.
- The separation of the deep trench from active areas determined by the STI edge is self-aligned and prevents stress arising from deep trench processing to interfere with active areas.
- The separation is determined by deep trench hard mask thickness (and possibly combined with STI stack height, i.e. depth of shallow trench).
- The trench localization is fixed and determined by the additional mask (trench mask).

- The additional mask is positioned on oxide spacer created for hard mask definition to accommodate for any misalignment (spacer width 2x gives an allowable misalignment of +/- x)
- Removal of oxide spacer after deep trench etch to allow for simultaneous corner rounding of deep trench and STI close to active area (bird's beak).

It will be obvious that the invention may be varied in a plurality of ways. Such variations are not to be regarded as a departure from the scope of the invention. All such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the appended claims.

CLAIMS

1. In the fabrication of an integrated circuit, particularly an integrated circuit for radio frequency applications, a method for forming shallow and deep trenches for isolation of semiconductor devices comprised in said circuit, characterized by the steps of:

- providing a semiconductor substrate (10);
- forming at least one shallow trench (18) by using a first mask (16) formed on said substrate, said shallow trench extending into said substrate;
- forming a dielectric layer (20) of a predetermined thickness (2x) on the structure obtained subsequent to the step of forming the at least one shallow trench;
- forming at least one opening (33) in said dielectric layer by using a second mask (22) formed on said dielectric layer and with an edge (30) of said second mask aligned to an edge (26) of said shallow trench with a maximum misalignment ($+/- x$) of half the predetermined thickness (2x) of said dielectric layer, said opening extending within the shallow trench to the bottom (18a) thereof, whereby a spacer (32) of a width equal to the predetermined thickness (2x) is formed in said shallow trench and along said edge thereof; and
- forming a deep trench (34) in said opening by using said dielectric layer as a hard mask, said deep trench extending further into said substrate and being self-aligned to said shallow trench.

2. The method as claimed in Claim 1, characterized by the step of choosing the predetermined thickness (2x) of the dielectric layer (20) and hence the distance between the edge (28) of said spacer, and thus of said deep trench (34), and the edge (26) of said shallow trench (18) in dependence on the semiconductor devices comprised in said circuit.

3. The method as claimed in Claim 1 or 2, characterized by the step of forming the dielectric layer (20) by conformal deposition, preferably chemical vapor deposition.

4. The method as claimed in any of Claims 1-3, 5 characterized by the step of forming a dielectric layer (14), particularly a silicon nitride layer, on said substrate prior to forming the at least one shallow trench (18).

5. The method as claimed in any of Claims 1-4, 10 characterized by the step of forming an oxide layer (12), particularly a thermal oxide layer, on said substrate prior to forming the at least one shallow trench (18).

6. The method as claimed in any of Claims 1-5, 15 characterized by the step of forming an oxide liner (36), particularly a thermal oxide liner, on the structure obtained subsequent to the step of forming the deep trench (34) in order to achieve corner rounding simultaneously at sharp edges of the shallow and deep trenches (18, 34), respectively.

7. The method as claimed in any of Claims 1-6, 20 characterized by the steps of depositing an isolation layer (38), preferably a TEOS layer, in the shallow and deep trenches (18, 34), filling said trenches with semiconducting (40) or insulating material and removing said semiconducting material from the shallow trench (18).

8. The method as claimed in Claim 7, characterized by 25 the steps of depositing an isolation layer (42), preferably a CVD or HDP oxide, in the shallow trench (18) and planarising the upper surface of said isolation layer.

9. The method as claimed in Claim 7, characterized by 30 removing said semiconducting material by the steps of planarising the semiconducting material by chemical mechanical

polishing, and etching back the semiconducting material from the shallow trench.

10. The method as claimed in any of Claims 1-9, characterized by that the semiconductor substrate (10) is of silicon.

11. The method as claimed in any of Claims 1-10, characterized by that the shallow trench (18) is formed by etching, preferably non-isotropic reactive ion etching.

10 12. The method as claimed in Claim 11, characterized by that the shallow trench (18) is etched to a depth (H) exceeding the thickness (2x) of the dielectric layer formed subsequent to the step of forming the at least one shallow trench.

15 13. The method as claimed in any of Claims 1-12, characterized by that the shallow trench (18) is formed to a depth of 0.2-0.7 μm from the silicon substrate surface (10a).

20 14. The method as claimed in any of Claims 1-13, characterized by that the dielectric layer (20) formed subsequent to the step of forming the at least one shallow trench is an oxide layer, preferably a TEOS layer, of a predetermined thickness (2x) of preferably about 1000-4000 Å.

25 15. The method as claimed in any of Claims 1-14, characterized by that the at least one opening (33) in said dielectric layer (20) formed subsequent to the step of forming the at least one shallow trench is formed by etching, preferably reactive ion etching.

16. The method as claimed in any of Claims 1-15, characterized by that the deep trench (34) is formed by etching to a depth of at least a few microns.

5 17. In an integrated circuit, particularly an integrated circuit for radio frequency applications, a semiconductor structure for isolation of semiconductor devices comprised in said circuit, characterized in that is fabricated by using the method as claimed in any of Claims 1-16.

10 18. In an integrated circuit, particularly an integrated circuit for radio frequency applications, a semiconductor structure for isolation of semiconductor devices comprised in said circuit, characterized in that it comprises a semiconductor substrate (10); at least one shallow trench (18) extending vertically into said substrate; a deep trench (34) laterally 15 within said shallow trench, said deep trench extending vertically further into said substrate, wherein said deep trench is self-aligned to said shallow trench with a controlled lateral distance between an edge of the shallow trench (26) and an edge (28) of the deep trench, and the lateral extensions of the 20 shallow and deep trenches, respectively, are independently chosen.

25 19. An integrated circuit, particularly an integrated circuit for radio frequency applications, characterized in that it comprises a semiconductor structure as claimed in Claim 17 or 18.

1/8

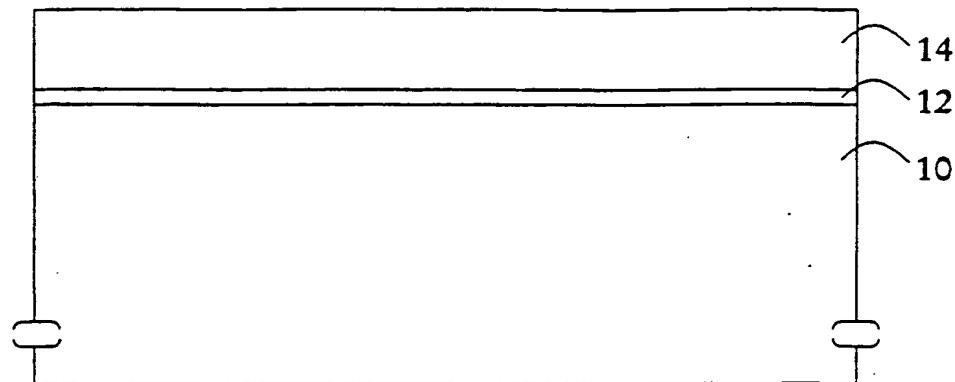


Fig. 1

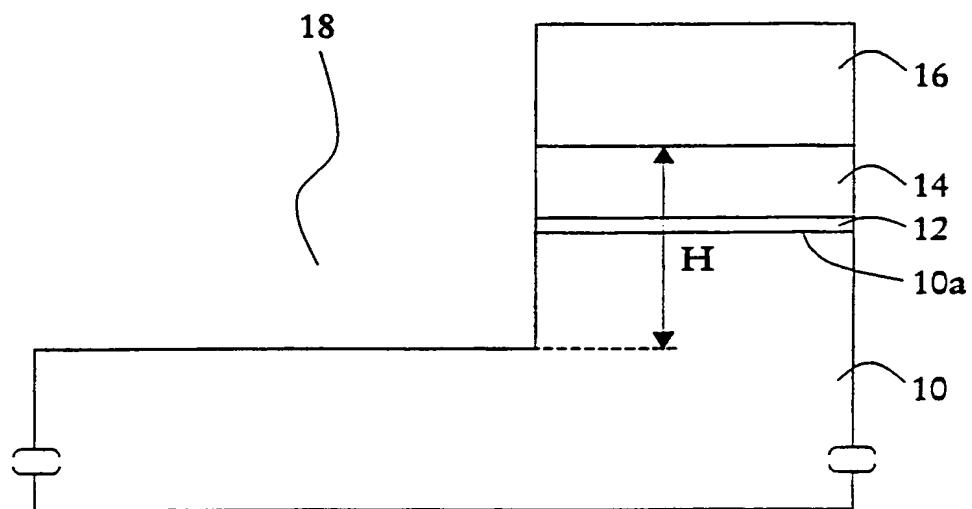


Fig. 2

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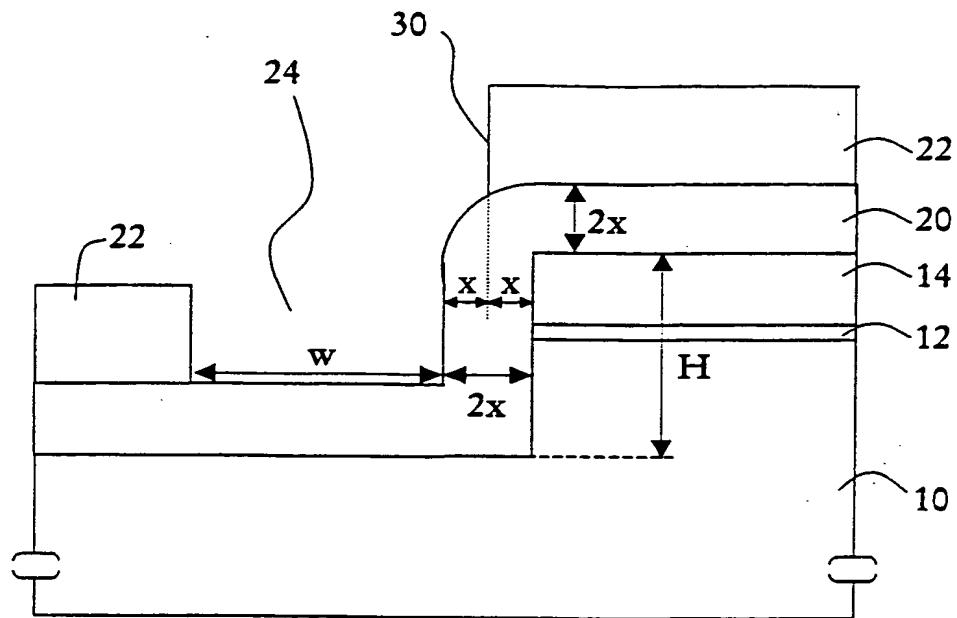


Fig. 3

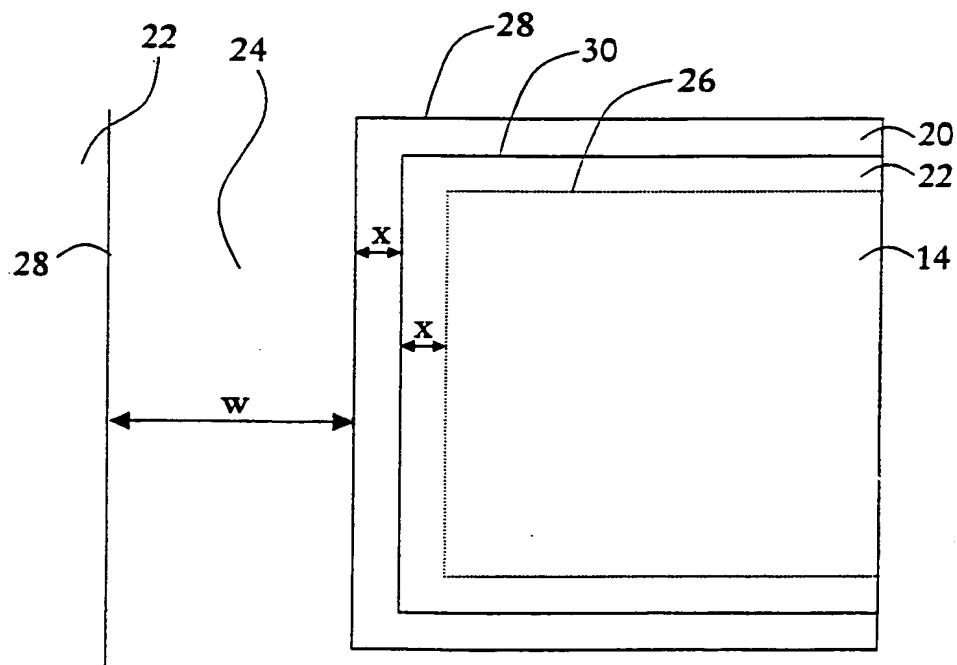


Fig. 4

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3/8

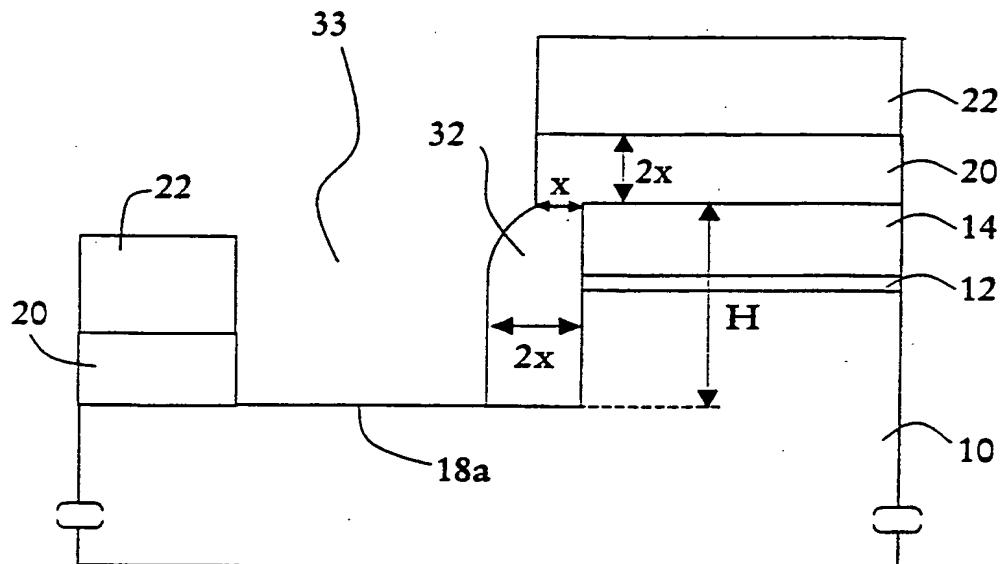


Fig. 5

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4/8

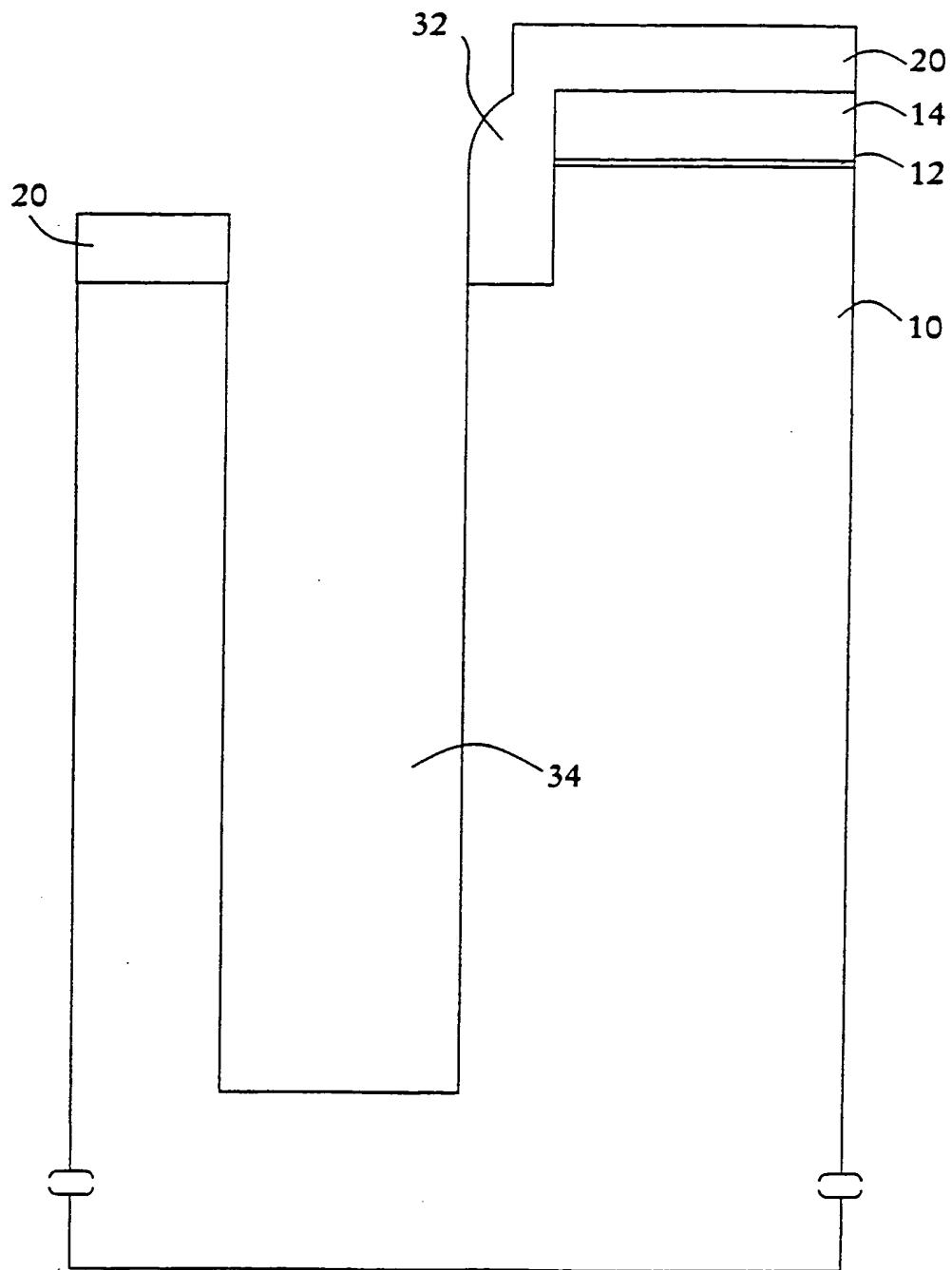


Fig. 6

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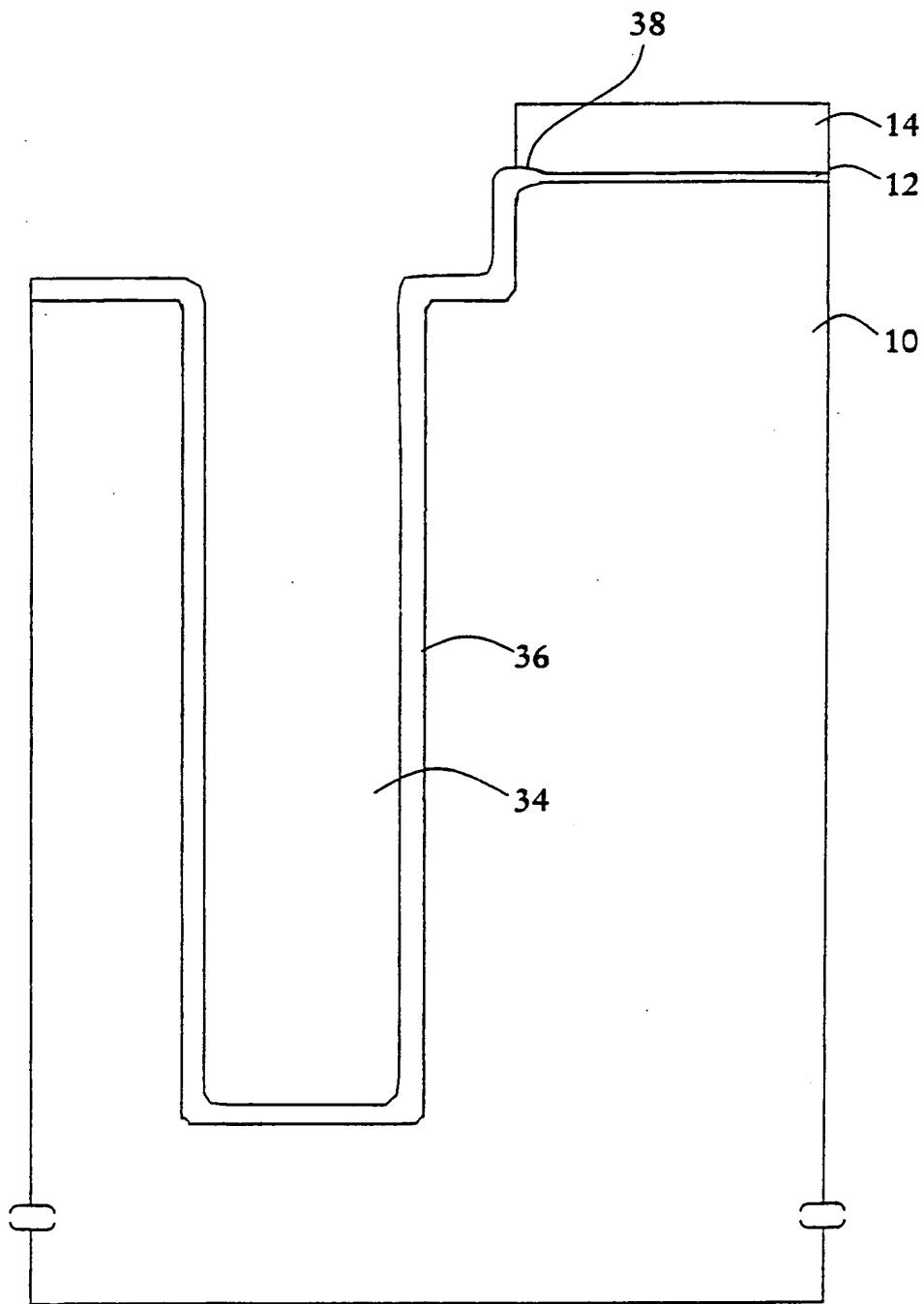


Fig. 7

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6/8

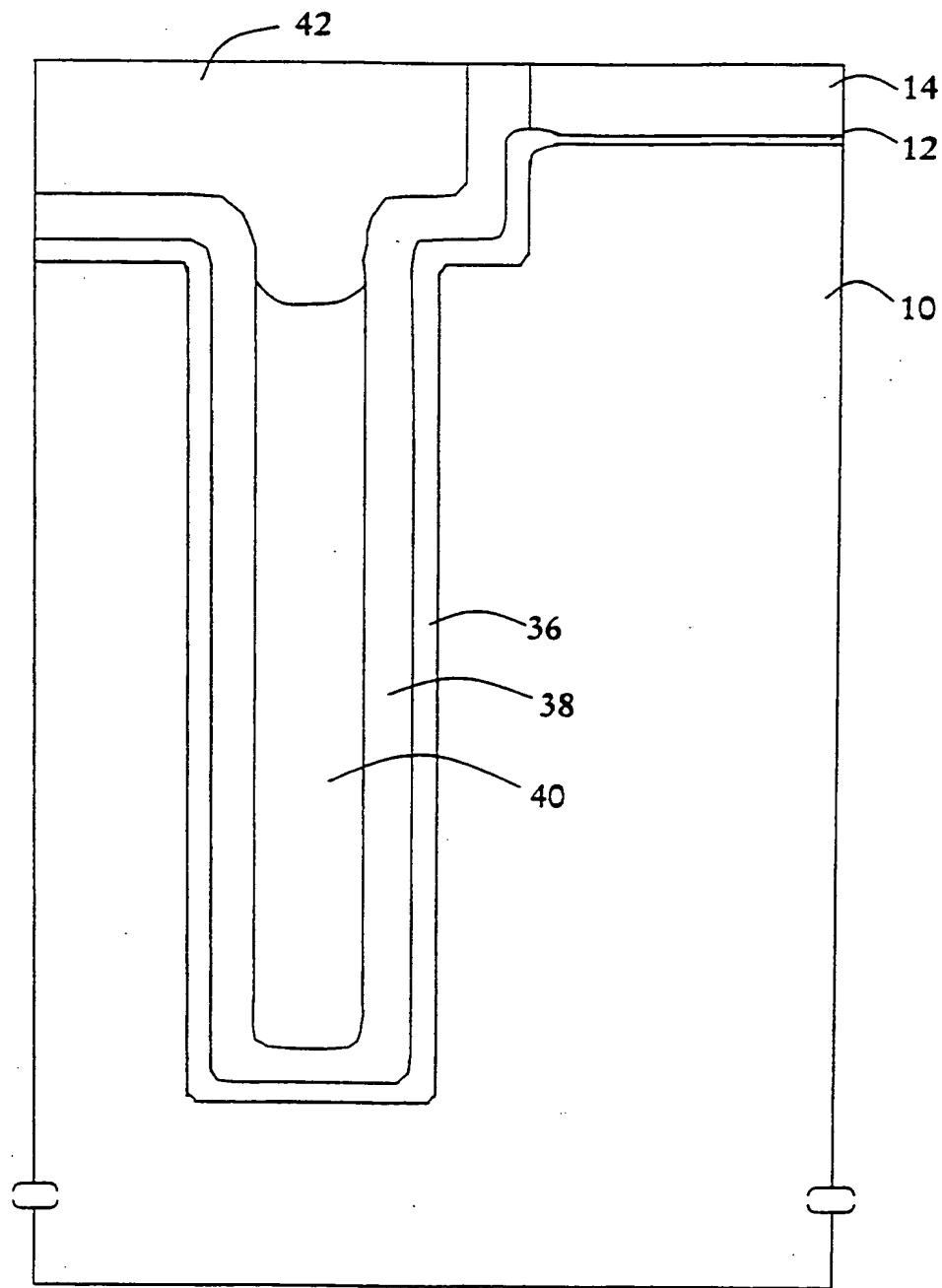


Fig. 8

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7/8

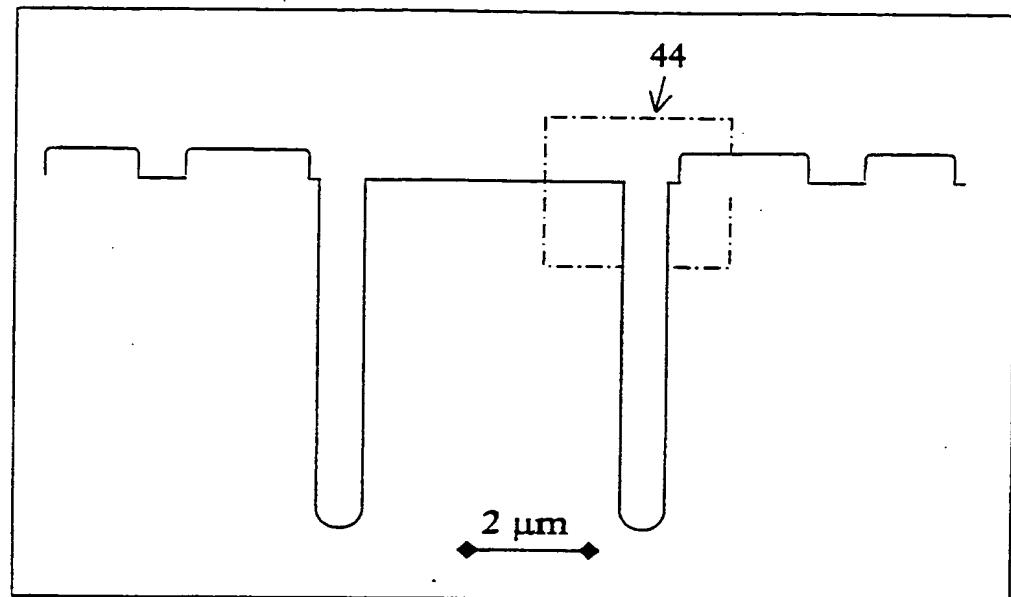


Fig. 9

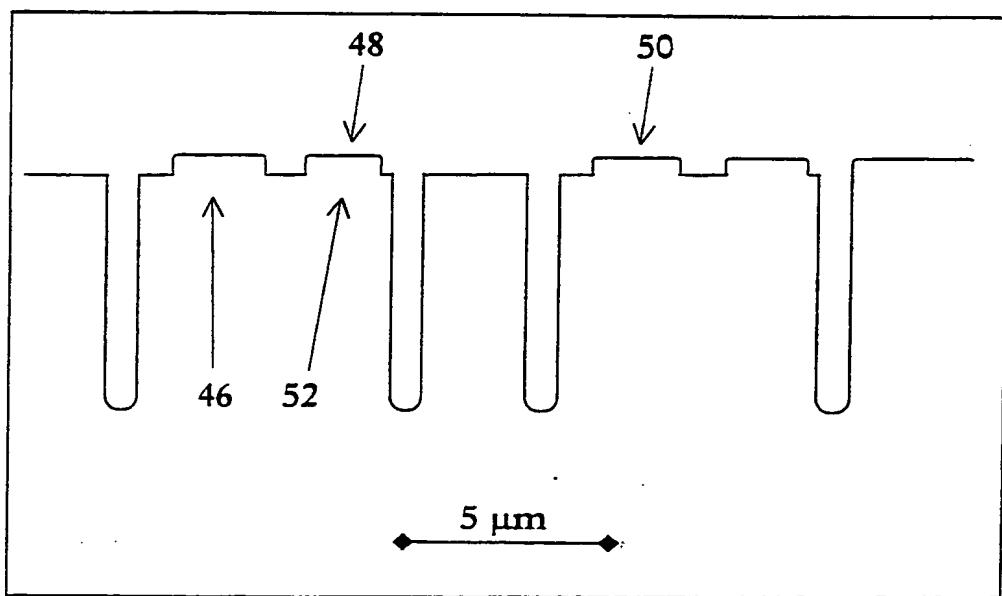


Fig. 10

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8/8

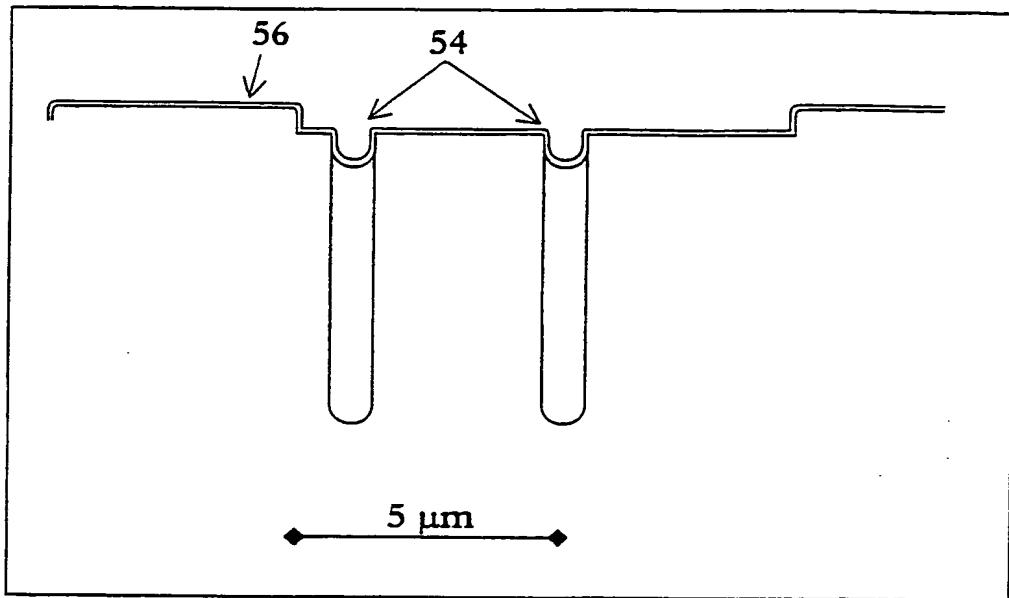


Fig. 11

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INTERNATIONAL SEARCH REPORT

International application No.

PCT/SE 00/01690

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: H01L 21/76, H01L 27/04, H01L 29/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5895253 A (SALMAN AKRAM), 20 April 1999 (20.04.99), column 4, line 37 - column 5, line 17, abstract	18-19
A	--	1-17
A	US 5536675 A (MARK T. BOHR), 16 July 1996 (16.07.96), column 4, line 64 - column 6, line 48, abstract	1-19
A	--	
A	US 5065217 A (DOUGLAS P. VERRET), 12 November 1991 (12.11.91), column 3, line 28 - column 4, line 47, abstract	1-19
	--	

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"P" document published prior to the international filing date but later than the priority date claimed

"I" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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Date of the actual completion of the international search

Date of mailing of the international search report

22 January 2001

23-01-2001

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 00/01690

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 9858406 A1 (VAN CLEEMPUT, PATRICK ET AL), 23 December 1998 (23.12.98), abstract --	8-10
A	US 5923993 A (SAHOTA S. KASHMIR), 13 July 1999 (13.07.99), abstract -----	8-10

INTERNATIONAL SEARCH REPORT

Information on patent family members

27/12/00

International application No.

PCT/SE 00/01690

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US 5895253 A	20/04/99	NONE		
US 5536675 A	16/07/96	NONE		
US 5065217 A	12/11/91	US 5298450 A		29/03/94
WO 9858406 A1	23/12/98	EP 0989930 A US 6109592 A WO 9857792 A		05/04/00 29/08/00 23/12/98
US 5923993 A	13/07/99	NONE		

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